An Integrated 3.125Gbps Ethernet Serial Transceiver in CMOS Technology

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Keywords: Ethernet; Transmitter; Receiver; Clock Generator; Line Driver; Phase Detector

Abstract. The design of a fully-integrated 3.125Gbps Ethernet transceiver is described. The circuit adopts parallel structure for both the transmitter and receiver to reduce the speed requirement. The transmitter uses multiphase clock to multiplex the data and current-mode line-driver to drive medium. The receiver uses 1/5-rate parallel-sampling clock and data recovery circuit to facilitate the design and eliminate the need of 1:5 demultiplexer. The circuit was design in 0.18μm CMOS technology. Simulations show that it works well for 3.125Gbps data rate with all process corners.

Introduction

The ever-increasing demand for bandwidth has pushed serial communication data rates over 10Gbps [1,2]. System integration, low cost and low power requirements have made CMOS the technology of the choice for serial transceivers. At present, the 10Gbps Ethernet can unity the network protocols among LAN, MAN and WAN [3]. There are two major challenges in high-speed links. The first is bandwidth of interconnection that limits transmitting data rate; the other is signal integrality that affects the actually operating robustness. In this paper, a reliable 3.125Gbps serial link transceiver in 0.18μm CMOS technology that is suitable for the IEEE 802.3ae 10Gigabit Ethernet applications is described.

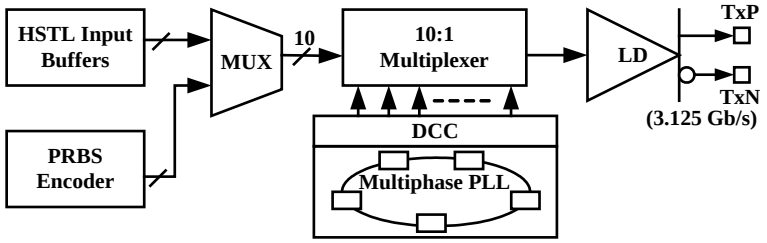
System Architecture

The transmitter architecture is shown in Fig. 1(a), mainly including multiphase clock generator, parallel-to-serial multiplexing circuit, current-mode linedriver and high-speed transceiver logic (HSTL) interface. The receiver shown in Fig. 1(b) accepts a 3.125Gb/s serial data stream, recovery the clock and data, and produces ten demultiplexed HSTL data outputs. It also includes byte alignment based on the comma symbol as defined in 8B/10B-encoded data. A 2^7-1 PRBS encoder and decoder are built on-chip for self test.

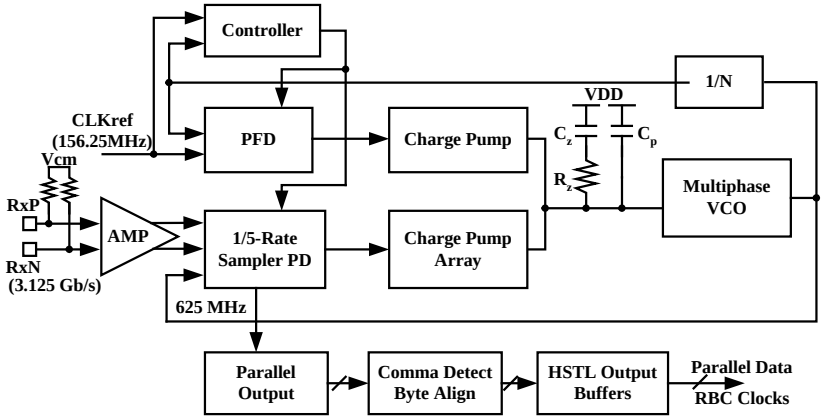
The receiver has two modes of loop operation: lock to reference clock for voltage-controlled oscillator (VCO) training; lock to data and deserialization for the normal mode. During power up or when the serial input data signal has been lost, the clock and data recovery (CDR) locks to the reference clock. Both loops share the VCO and loop filter. The oscillation frequency of the VCO is 1/5 times lower than the data rate so that the VCO can provide sufficient turning range and tolerate the temperature and process variations efficiently.

At very high data rate, accurate phase measurements are extremely difficult to achieve with reasonable power, and circuit imperfections cause the linear Hogge phase detector to deviate from the ideal characteristic. The bang-bang phase detector outputs only signify whether the clock is early or late with respect to the ideal sampling instant. This early/late PD-based PLLs are quasi-digital systems and consequently they are more resistant to component and process variation as well as noise. In addition, an early/late PD possesses intrinsic matching between the sampling and retiming phases, providing simplicity in design and better phase adjustment at high speeds. It is this combination of robustness, speed, and simplicity in parallel design for which the bang-bang CDR was used in this design.

  DOI: 10.25236/icicta.2019.003



(a) Transmitter



(b) Receiver

Figure 1. Block diagram of the (a) transmitter and the (b) receiver

Circuit Design

A. Multiphase Clock Generator

Charge pump PLL with ring oscillator is used to generate on-chip ten evenly spaced clock phases, which is used for high-speed data multiplexing in transmitter and phase sampling in receiver. The voltage-controlled oscillator (VCO) is a five-stage ring oscillator based structure. One of the delay stages and the bias voltage generator are shown in Fig. 2. It is designed to have high supply noise immunity while being able to operate at low supply voltages. The key components to achieve these objectives are the symmetric load elements and the self-biased replica-feedback current source bias circuit [4].

The duty cycle of clock signals within the multiphase PLL deviates from its ideal value (50%) due to various asymmetries in signal paths and mismatches in device parameters. For applications in which the timing of both edges of the clock is critical, the clock buffer with duty cycle correction (DCC) function is required to maximize timing margins. The DCC buffer is configured as an offset corrector stage with an extra feedback duty detector stage to correct the duty-cycle error of output clocks.

The VCO oscillation frequency can be expressed as

$$f_{VCO} = \frac{\mu_p C_{ox} (W/L)_s (V_{DD} - V_{CTRL} - |V_{TP}|)}{\lambda C_B} \tag{1}$$

where $(W/L)_s$ is the device parameter of one of the PMOS transistors in symmetric load, C_B is the total output capacitance for all stages, and λ is a proportional coefficient related to oscillator structure. Taking the derivative with respect to V_{CTRL}, the VCO gain K_{VCO} is given by

$$K_{VCO} = \left| \frac{df_{VCO}}{dV_{CTRL}} \right| = \frac{\mu_p C_{ox} (W/L)_s}{\lambda C_B} \tag{2}$$

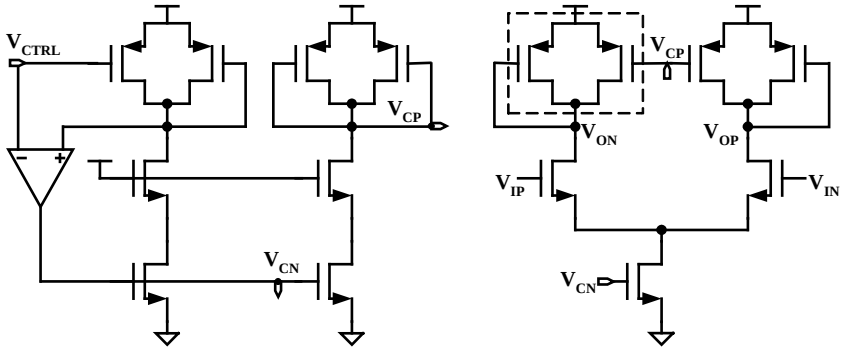


Figure 2. Bias voltage generator and delay cell

B. Multiplexer and Line driver

Because maximum operating speed of parallel-to-serial circuit with shift register type is often limited by on-chip clock speed, the parallel multiplexing architecture shown in Fig. 3 is adopted to overcome this speed limitation. Instead of using pass-transistor switchers, the 10:1 multiplexer consists of 10 pseudo-NMOS modules, each made of stacks of NMOS transistors which accepts two phases of the clock that are a symbol period apart and qualified by pre-driver AND gates. The current mode linedriver is chosen for good immunity to ground and power supply noise that improves signal integrality of the transmitter. Fig. 3 shows a fully differential implementation with on-chip line impedance matching and output amplitude controlling.

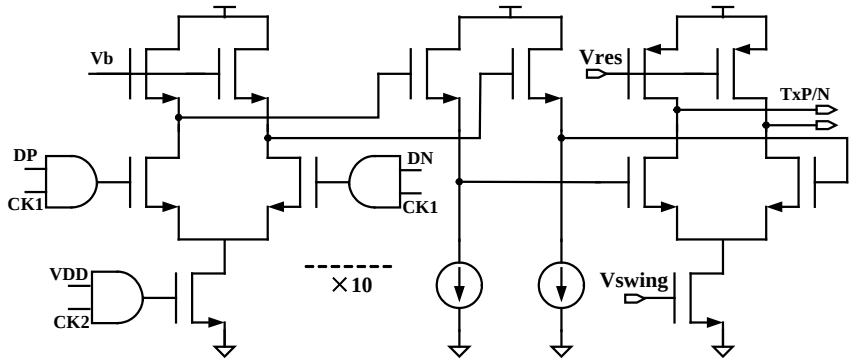


Figure 3. 10:1 multiplexer and line driver

C. Data phase detector

Fig. 4 shows the block diagram of the proposed 1/5-rate data phase detector and its multi-branch charge pump. It employs the 2x oversampling [5] and operates at 1/5 of the input serial data rate. The ten parallel samplers are gate-isolated sense-amplifier-based flip-flops (SAFF). Using equally spaced 625-MHz 10-phase clocks CK0-9, five bits of input data are sampled in parallel and each serial bit is sampled two times. Every three consecutive samples are used for transition detect and phase comparison. During the data transition, if the edge sample has the same logic level with the previous data sample, then the clock is early otherwise the clock is late [6]. In absence of data transition, the tri-state charge-pump control provides a hold mode in the PLL filter to reduce jitter generation. When the phase is locked, the data samples D1-5 latch the data at the center of the data eye; the edge samples E1-5 are timed to the data transitions. In order to deal with the independent parallel operation, the improved charge pump has five-pair time-interleaved current branches with shared current source, as shown in Fig. 4.

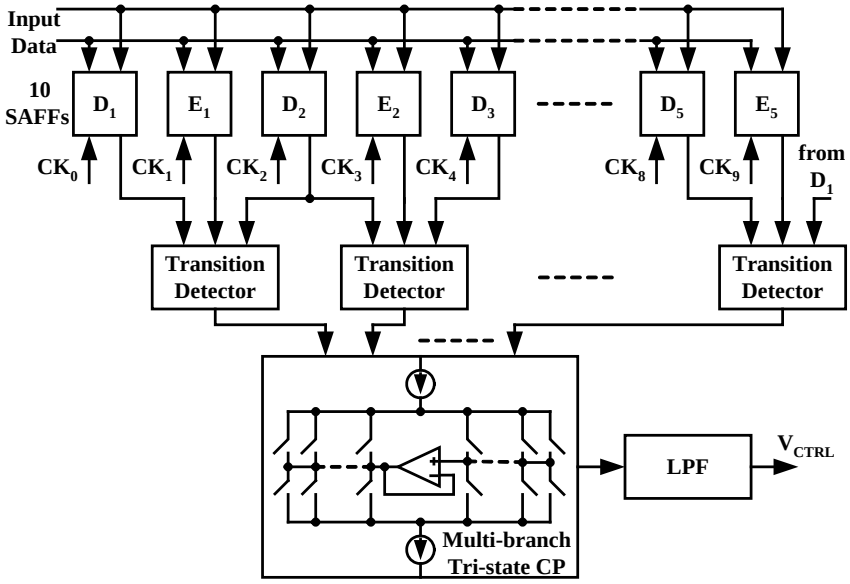


Figure 4. Phase detector and multi-branch charge pump

D. Charge pump constant-gm bias circuit

In order to get a nearly constant unity-gain bandwidth and phase margin of PLL in different PVT (process, voltage, and temperature) corners, a current biasing circuit shown in Fig. 5 is used in charge pumps. It consists of constant-gm bias loop [7], high-swing cascode bias circuit and start-up circuit.

In Fig. 5, around the loop consisting of M_1, M_2 and R, and applying the voltage-current relationship in MOS transistor, we have

$$\sqrt{\frac{2I_{D2}}{\mu_p C_{ox}(W/L)_2}} = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_1}} + I_{D1}R \tag{3}$$

Assuming that $I_{D1} = I_{D2} = I_{CP}$ due to the current-mirror pair M_5-M_6 and M_3-M_4, and for the special case of $(W/L)_1 = 4(W/L)_2$, (3) can be written as

$$I_{CP} = \frac{1}{2\mu_p C_{ox}(W/L)_2 \bullet R^2} \tag{4}$$

Multiplying (4) with (2), we can get

$$I_{CP} \bullet K_{VCO} = \frac{(W/L)_s}{2\lambda \bullet (W/L)_2 \bullet R^2 C_B} \tag{5}$$

Thus, on the first order this value is determined by geometric parameters only, independent of power-supply voltages, process parameters, and temperature. Because of the direct relationship with the resistor value, the resistor R is designed can be adjustable from the on-chip SCI (serial control interface) circuit.

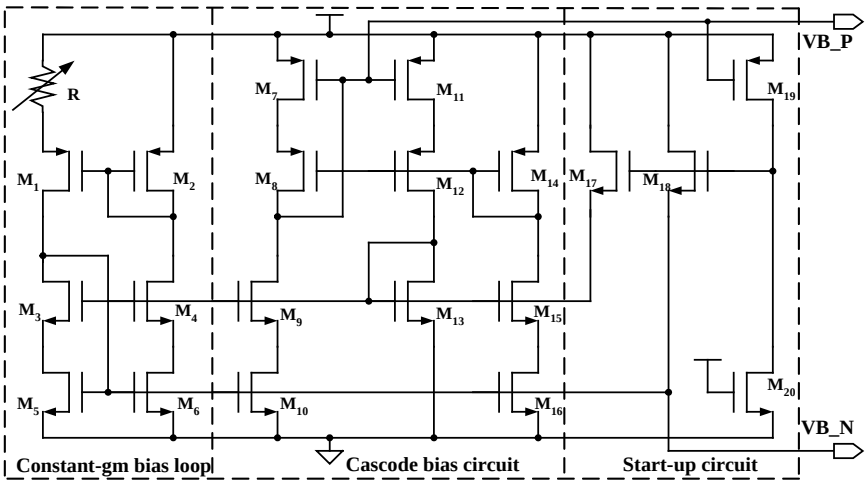


Figure 5. Charge pump biasing circuit

Simulation Results

The circuit is designed in 0.18μm CMOS technology and simulated by Cadence Spectre under all process, voltage, and temperature (PVT) variations. The low-pass channel effect and package model are included in this simulation. Additionally, switching noise is modeled by injecting a square wave into the power supply. Simulation results show that the circuit works well for 3.125Gbps data rate with all technology corners and temperature varies from 0°C~125°C.

Fig. 6 shows the simulated outputs of the multiphase clock generator and transmitter data eye at 3.125Gbps. The transmit data eye with 2^7-1 PRBS pattern has a total jitter of 45ps (peak-to-peak) and its differential output voltage swing is 1600mV. Fig. 7 shows the simulated eye diagrams of the received data at 3.125Gbps and the recovered clock at 625MHz. The recovered clock frequency is 1/5 of the data rate and has a peak-to-peak jitter of 75ps. Of the recovered clock jitter, some is due to the power supply noise, and most of the remaining jitter arises from the mismatch in charge pump and bang-bang operation. We expect the jitter will be minimized by further design and lowing the loop bandwidth. But the latter may be conflicting with the jitter tolerance performance.

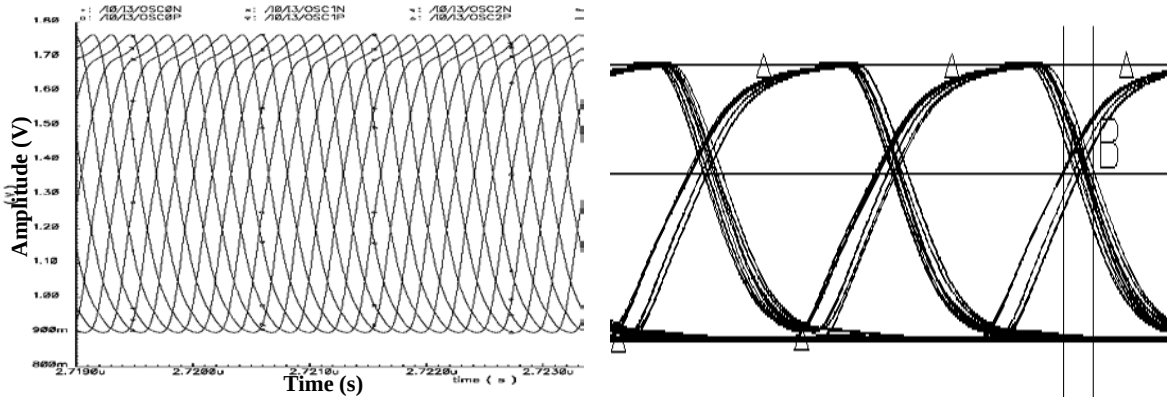


Figure 6. Simulated multiphase clocks and transmitted data eye

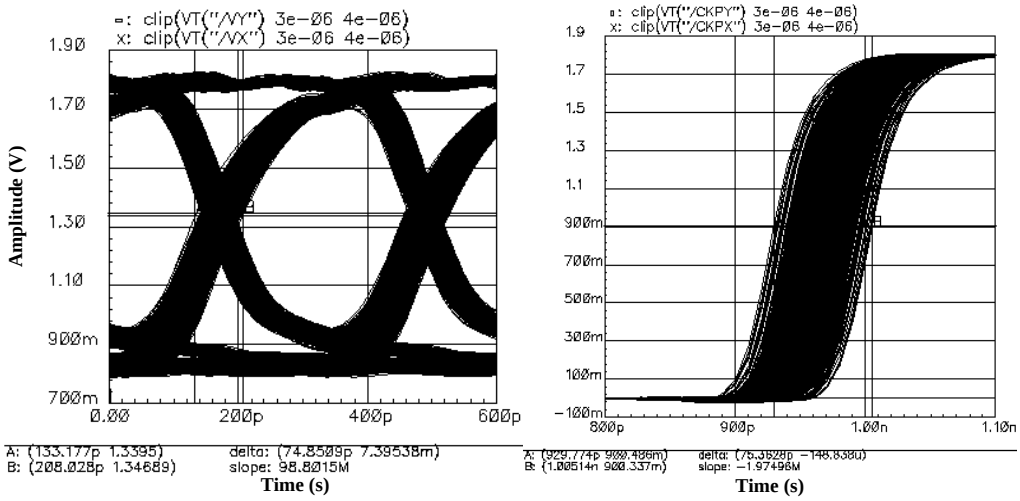


Figure 7. Simulated eye diagram of the received data and recovered clock

Summary

A 3.125Gbps transceiver in CMOS technology for IEEE 802.3ae multichannel 10Gbase Ethernet interface is described. Employing the multiphase VCO with duty-cycle correction, parallel pseudo-NMOS AND multiplexing with current mode line-driver, 1/5 rate clock and data recovery circuit with parallel sampling technique, constant-gm biasing circuit for charge pump, and HSTL interface buffers, it achieves the reliable 3.125Gbps operation under all technology corners. In typical conditions, the core circuit dissipates 100mW in transmitter and 95mW in receiver from a single 1.8V supply. The serial transceiver realizes the low power, low cost and compact solutions for the exponential need of broadband network application.

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